# AB35

## Implementing Large and Non-Standard Transforms

Application Brief

AB35 - 1.0 February 1994

### BACKGROUND

The PDSP16510 is a stand-alone FFT Processor which performs 16, 64, 256, or 1024 point FFT's with input sampling rates of up to 40MHz - typically an order of magnitude faster than programmable DSP parts. A single device can window and transform up to 1024 complex points without the need to access external memory during the computation. The device internally uses 16 bit block floating point arithmetic, which provides sufficient precision to allow transform sizes of 4096 points, or even 16384 points in some circumstances, to be implemented with adequate dynamic range.

The purpose of this application note is to describe how the PDSP16510 can be used in systems requiring transform sizes of up to 16384 complex points. In such applications it is necessary to support the PDSP16510 with other arithmetic devices from the PDSP family. Several alternatives are presented but the optimum architecture has a regular structure, is easy to control, and can be repeated as required to accommodate high input sampling rates.

### DOING 512 POINT TRANSFORMS

Before going on to consider transform sizes of greater than 1024 points, the special case of the 512 point transform will first be considered. The radix 4 algorithm used by the PDSP16510 requires that the transform length be a power of four, so how can this be modified to handle 512 points?

The simplest way is to zero pad the input data, perform a transform of twice the required length and then discard half the spectral results. There are, however, two possible ways of inserting the zero's; either an equal number of zeros as data points can be appended to the end of the data block or a zero can be inserted between each data point. Appendices A and B present the mathematics of both these techniques, but in order to exploit the window and overlap facilities of the PDSP16510, it is essential to use the interleaving zero approach.

Rember that the PDSP16510 will apply its internal window operator to the complete 1024 point block, and not just to the 512 samples of actual data. Thus, if all the zero's are appended at the end, the data will be incorrectly modified since the actual data will only use half the window operator. In fact if block overlapping is used there will be a phase shift in the results, even for the case of a rectangular window. By interleaving with zero's, the actual data will be modified by every other value in a window containing 1024 operators. This is the correct value for 512 samples using a window with 512 operators.

In the case of interleaving zero's Appendix B proves that the spectrum is repeated in the second half of the outputs. Thus, even though a 1024 point transform is calculated, only the first 512 results need be outputed. The PDSP16510 provides an option to only output half the results, and hence improve the efficiency of the calculation. When zero's are appended at the end, the required spectrum is contained in the even results. The PDSP16510 does not provide an option to output only even results.

A suitable hardware configuration for performing 512 point transforms is shown in Figure 1. The PDSP16540 Bucket Buffer is needed to support continuous transforms, and also to implement block overlapping. Data is written to the buffer at twice the

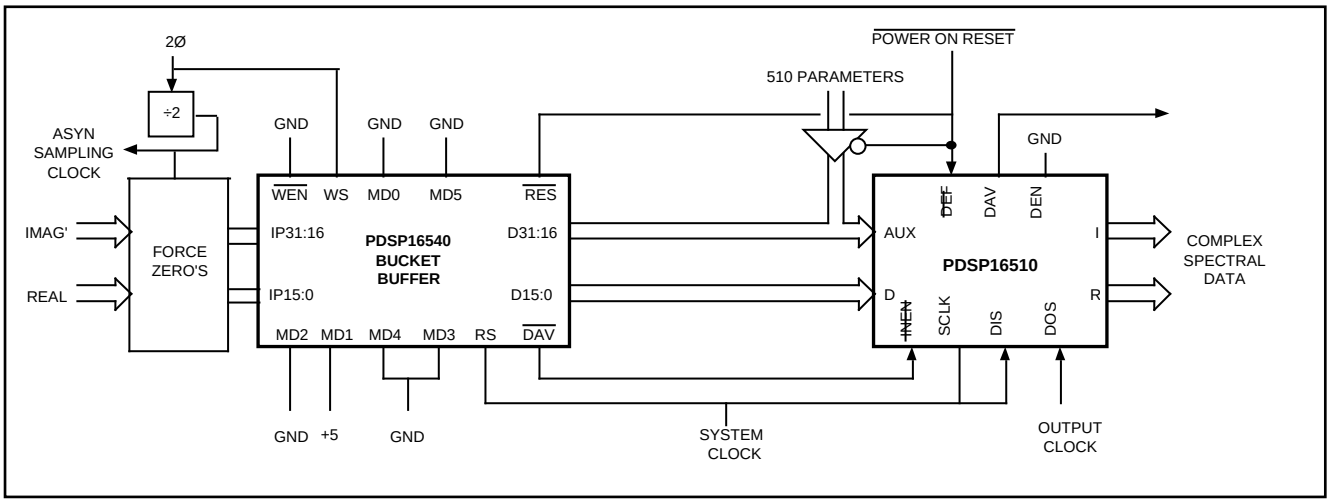


*Figure 1. System for Performing 512 Point Complex Transforms*

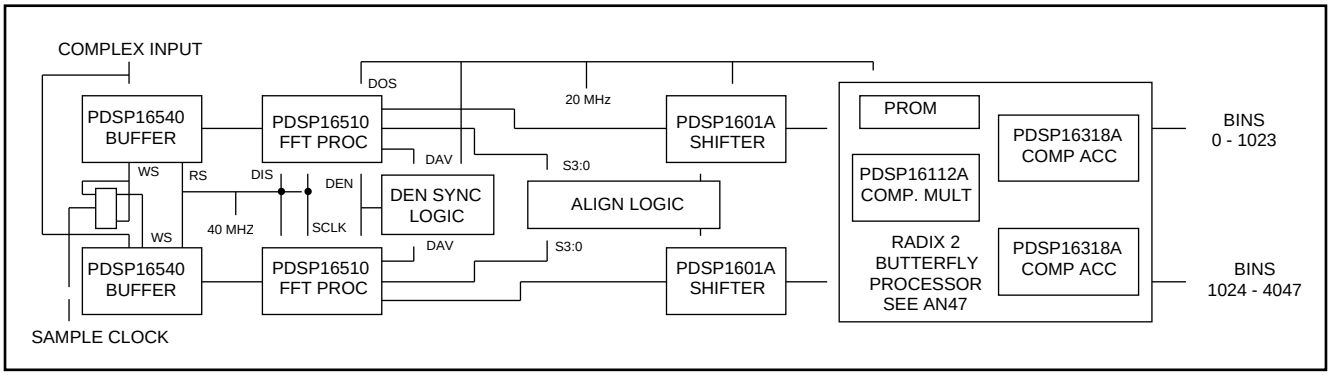


*Figure 2. The Direct way to Implement 2048 Point Complex Transforms*

original sampling rate, with external logic inserting zero's during the odd clock periods. Such a configuration will support a maximum data sampling rate of 3.4 MHz, but this can be increased to 20 MHz by connecting six devices in parallel. This multiple device arrangement is described in the PDSP16510 data sheet, and it should be noted that the Bucket Buffer is then not needed. The sampling rates achievable with a given number of devices will always be half those obtainable when doing true 1024 point transforms.

This highlights the disadvantages of the zero's insertion technique; the continuous sampling rates achievable are only half those obtainable when doing straightforward transforms of the same length. This stems from the fact that in the time taken to complete the whole transform operation, only half as many actual samples must have been written into the input buffer. Other system constraints must thus have dictated the need to only do 512 point transforms, rather than the transform time itself.

The techniques described in the following sections indicate how large transforms can be implemented, and are also applicable to 512 point transforms. In essence they trade the simple parallel approach to increasing the sample rate with additional multipliers, PROMS, and accumulators.

**THE DIRECT WAY TO IMPLEMENT LARGE TRANSFORMS**

Equation 1 in Appendix A indicates that an N point DFT can be expressed as the summation of the even and odd, N/2 point, DFT's; in fact a summation of the even points and the odd points twiddled by the otherwise missing sine and cosine values. Appendix A goes on to show that Equation 1 only represents the first half of the N point DFT. The second half is shown to be obtained by a twiddle and difference operation.

The direct way to implement a 2048 point transform would thus be to use two PDSP16510's; one performing a 1024 point transform on the odd inputs, and the other performing a 1024 point transform on the even inputs. As shown in Figure 2, the addition of a PDSP16112 complex multiplier and two PDSP16318 complex accumulators will combine the results to simultaneously produce both halves of the 2048 point transform. The use of the PDSP16540 Bucket Buffer allows the incoming data to be continuous, and any amount of block overlapping can be selected.

In this system both PDSP16510's must produce their results simultaneously. This can only be gauranteed if the outputs are controlled by the DEN input. When both DAV outputs have gone valid, a DEN signal should be produced which is synchronized to the DOS strobe. The even sequence will then be exactly concurrent with the odd sequence, once the output circuit has been primed ( see the DSP Handbook page 134 ). If the derived DEN signal is delayed by 14 DOS strobes ( 4 PDSP16510 priming delays plus 8 PDSP16112 delays plus 2 PDSP16318 delays ) it can be used to provide a Data Valid signal to the rest of the system.

One of the complex accumulators can be avoided if the results produced by the PDSP16510's are read twice, firstly to produce bins 1-1023 with an add operation, and then bins 1024 - 2047 with a subtract operation.

This configuration has two shortcomings; the internal window operator cannot be used and shifters are required to align the

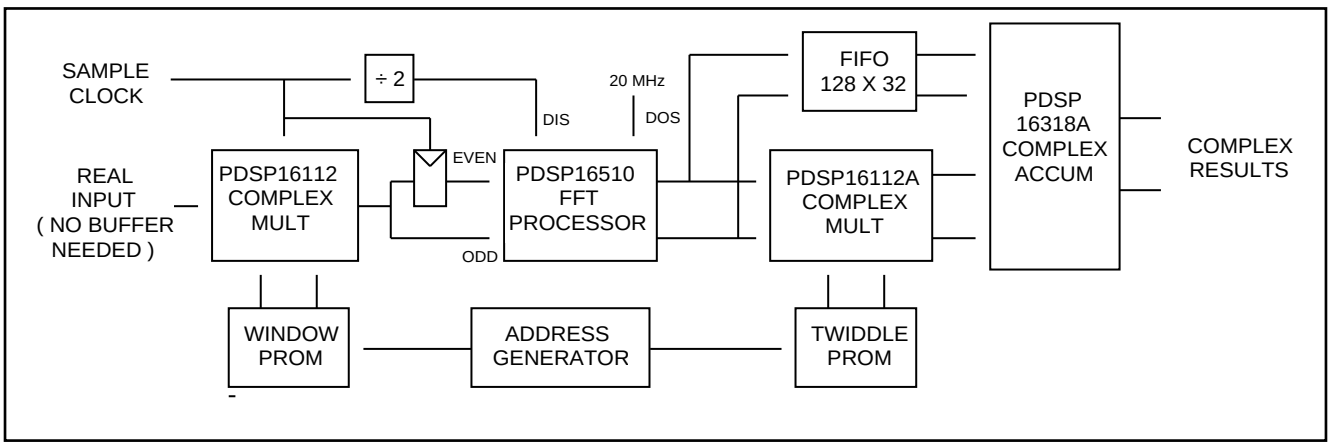


*Figure 3. A System to do 512 Point Real Transforms*

outputs from the PDSP16510's. The system thus needs an additional complex multiplier to window the data, which cannot be combined with the post twiddle operation needed in the backend butterfly processor. This is not shown in Figure 2. The shifters are needed since it cannot be guaranteed that both devices will produce the same block exponent from the internal variable shift operation, and turning this feature off would produce very poor dynamic range. PDSP1601's can be used for the shift operation, but unfortunately they have to be positioned before the combination of the results, and four devices are needed to shift two sets of 32 bit outputs. More efficient configurations are discussed in the next section.

This direct approach to computing larger transforms can, however, be used to produce an efficient system for 512 point real transforms. Such a system is shown in Figure 3, which illustrates a PDSP16510 configured to perform two simultaneous 256 point real transforms. This system will support incoming sampling rates of up to 19.5 MHz when doing 512 point real transforms ( see Table 5 in the datasheet ). With 50 % overlapping the rate reduces to 9.7 MHz, and with 75% overlapping it reduces to 4.8 MHz. To support these input rates the output rate should be at least equal to 19.5 MHz sampling rate. Since the PDSP16510 would need a 40 MHz system clock to achieve these throughputs, a convenient solution would be to divide this clock by two and then to use it as the output strobe. Both the PDSP16318A and PDSP16112A will support output clock rates of 20 MHz.

In this system the even samples are applied to the real input pins of the FFT Processor, and the odd samples to the auxiliary pins. No output shifters are needed since both sets of outputs will be internally shifted by the same amount. Since the PDSP16510 will output all the even results followed by all the odd results, it is necessary to buffer the even results in a FIFO. As the odd results are outputed they are twiddled and added to the even results coming from the FIFO.

In the case of real transforms the second half of the spectrum is a repeat of the first half. Thus the PDSP16510 will only output 128 even bins followed by 128 odd bins, even though two sets of 256 samples were applied. Only one PDSP16318 is needed at the output doing a complex add operation; the second half of the results do not exist and the twiddle and subtract is not needed.

This system can use the internal block overlapping features of the FFT Processor. Unfortunately the internal window operator cannot be used, and to perform this function a complex multiplier is needed at the input as shown in Figure 3.

**MORE EFFICIENT WAYS OF IMPLEMENTING LARGE TRANSFORMS**

Appendix C shows how an N point DFT can be performed by a combination of L and M point DFT's where N = L x M. After the L point transform the results are twiddled by $\exp(-j2\pi ms/N)$ where m = 0 to M-1, and s is the row index. So how should L and M be chosen to make optimum use of the PDSP16510 and its supporting devices?

The most obvious approach is to use two FFT Processors, with an intermediate memory to store the results from the column transforms, and a complex multiplier to apply the intermediate twiddle factor. But this solution has three drawbacks; the memory cannot be a simple FIFO, since an address translation from columns to rows is needed, the internal window operators cannot be used, and results from the column transform will have different scaling factors. The last problem can be avoided by restricting the column transform to 16 points and turning off the internal block floating point option. With such a small transform size the dynamic range should not be compromised, and with the second FFT Processor doing 256 point transforms the system would handle 4096 points. In such a system, however, the window operator can only be applied to the data before it is stored in the input buffer. Thus the system needs two additional complex multipliers, one for the window operator and one for the intermediate twiddle.

This requirement leads to the possibility of making better use of the complex multipliers. Rather than using two PDSP16510's why not make the columns very small and use a complex multiplier and accumulator to perform a straightforward DFT, rather than an FFT? Thus a 2048 point transform can be done by calculating a 2 point DFT followed by a 1024 point FFT. The calculation of a 2 point DFT requires no multiplications, and the window and intermediate twiddles can be combined into one multiply operation.

We have thus chosen L in Appendix C to be 2, and M to be 1024. The row index, s, is thus 0 or 1. The data is thus arranged with samples 0 - 1023 in one row and 1024 - 2047 in the other row. **One** point of each of the two point DFT's is then calculated using samples 0 and 1024, followed by 1 and 1025, up to 1023 and 2047. The even point DFT calculation is just the sum the two inputs, and, since s = 0 in the first row, then the intermediate twiddle is unity . The resulting data is loaded into the PDSP16510,

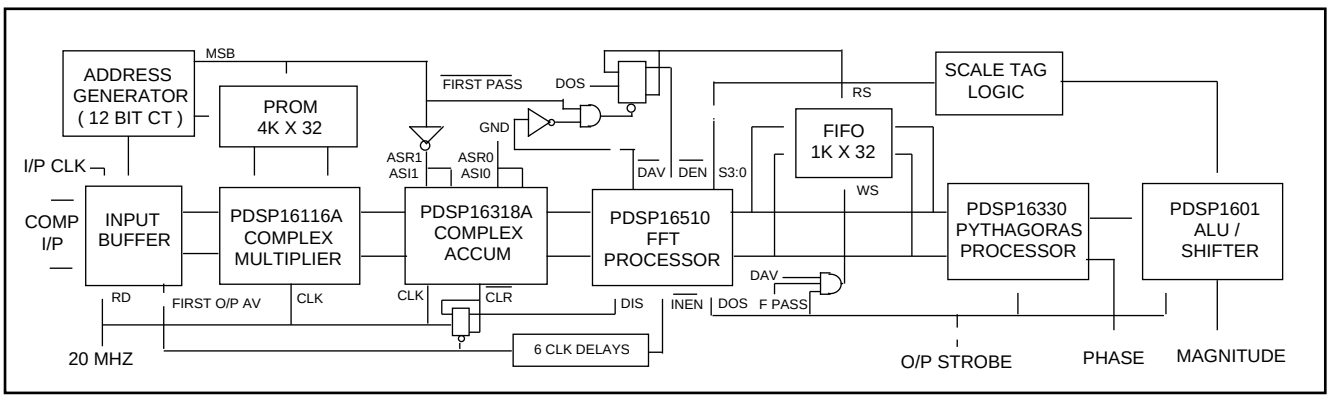


*Figure 4. An efficeint system for performing 2048 Point Transforms which can adapted for up to 16384 Points*

which does a 1024 point transform to calculate the even results of the 2048 point transform that is required. Since the twiddle values are unity, the PROM should contain the unmodified window operators which are read in the same sequence as the data from the input buffer i.e. 0, 1024, 1, 1025 etc.

The second point of the two point DFT is now calculated, and is simply the difference of the same sequence of values used previously. These must then be twiddled by exp( -j2πm/2048 ),before being transformed by the PDSP16510 to produce the odd values of the 2048 point transform. This can be done prior to the DFT by storing a second set of window values in the PROM which have been modified by these twiddle factors.

A system which will perform the necessary calculations is shown in Figure 4. The input buffer must handle any necessary block overlapping, and must allow sample 0 to be read out first, followed by sample 1024, then sample 1 and so on. The PDSP16116A performs the necessary complex multiplication using values from the PROM. The PROM must contain a set of 2048 window values plus a second set of modified window values as previously explained. A simple 12 bit counter can be used to provide the address sequences, with the most significant bit providing a page address bit, and the least significant bit used to provide the most significant address bit in each page.

The DEN and FIFO read strobe logic, shown in Figure 4, assumes that the odd results are calculated first. These are then dumped as quickly as possible into a FIFO. The outputs from this FIFO can then be mixed with the even results as they are produced by the FFT Processor during the next pass. The DEN pin on the PDSP16510 can be used to cause its outputs to go high impedance on alternate DOS output strobes. The real and imaginary complex outputs for the PDSP16510 can be converted to magnitude and phase by the PDSP16330 Pythagoras Processor.

The PDSP16318 does a complex subtraction whilst the first set of intermediate values are read into the PDSP16510, and then does an addition for the second set of inputs. Since the arithmetic could generate a 17 bit result, it is necessary to set the shifter within the PDSP16318 such that the 16 output pins for each complex component discard the least significant bit from the accumulator ( S2:0 = 011 ).

The sequence of events within the PDSP16318 is as follows, and produces an input for the PDSP16510 on every other clock cycle ( after an initial delay of 3 clock cycles ).

1) Load complex point A0. Clear the accumulator (after the next clock edge )
2) Load complex point B0. Transfer A0 to the accumulator ( ALU function is Accumulator + A0 )
3) Load point A1, Clear the accumulator ( after the next clock edge ). Do Accumulator + B0 and load the output register.
4) Load point B1. Transfer A1 to the accumulator. A0 + B0 available at the output pins.
5) Load point A2. Clear the accumulator etc

The two sets of outputs produced by the PDSP16510 will have different bit significance, as indicated by the Scale Tag values. This tag indicates the number of left shifts which have occurred in order to compensate for too many right shifts introduced to prevent possible overflow in the internal data path. Thus a smaller scale tag indicates a larger output number. To preserve dynamic range it is necessary to keep the larger set of results, thus the results with the larger scale tag value must be shifted right ( divided by 2 ) by the difference in the scale tag values. This can be done using the barrel shifter within a PDSP1601 ALU. This normalization is best done on the 16 bit magnitude output from the PDSP16330, since the phase outputs will always be correct without any shifts.

The same arrangement can be used to calculate transforms of 4096 points if the PDSP16116 and PDSP16318 are used to generate **each point in turn** of a 4 point DFT. Similarly 8192 points can be transformed if each point of an 8 point DFT is

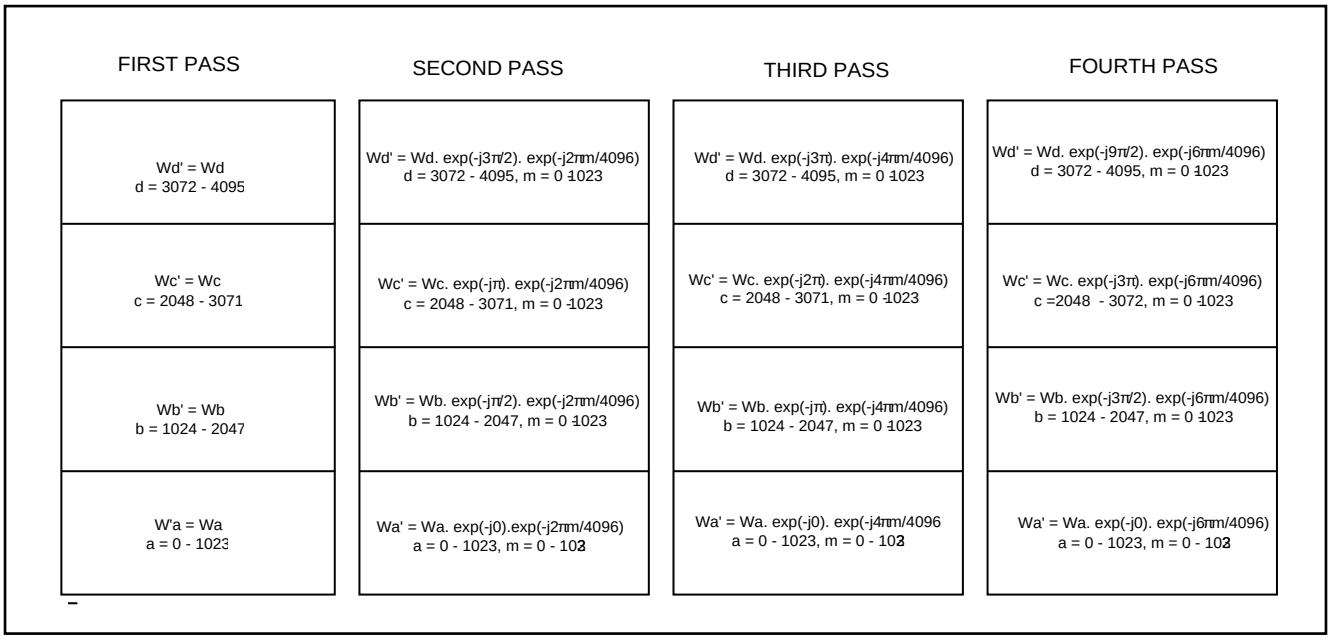


*Figure 5. Modified Window Operators needed to perform 4096 point Transforms with one external multiplier*

calculated, and16384 points can be transformed if 16 point DFT's are done. This will be illustrated using a 4096 point transform.

The original 4096 samples must be arranged in four rows, each containing 1024 columns. Thus Row 0 contains samples 0 - 1023; Row 1 contains samples 1024 - 2047; Row 2 contains samples 2048 - 3071; and Row 3 contains samples 3072 - 4095. To begin the complex multiplier / accumulator calculates the first value in the 4 point DFT using samples 0, 1024, 2048, and 3072. It then calculates the first value using samples 1, 1025, 2049, and 3073 and so on until the first points of all 1024 four point DFT have been calculated.

From the DFT equation given in Appendix A, each value is calculated by a twiddle and summation of the four inputs. The twiddles are expressed as $\exp( -j2\pi kn/4)$ where n is 0, 1, 2, or 3 for the four samples selected, and k = 0 for the calculation of each of the first points or X(0) values. Thus for the trivial case when k = 0;

$X(0) = x(0) + x(1024) + x(2046) + X(3072)$ where X(0) is the first intermediate DFT value.

This calculation is repeated using samples 1, 1025, 2049, and 3073 etc. and the 1024 results are applied to the PDSP16510. This produces results which represent bins 0,4, 8,12 etc. in the 4096 transform actually required.

X(1), X(2), and X(3) must then be calculated using the same groups of 4 inputs, using k = 1 for the calculation of X(1), k = 2 for the calculation of X(2), and k = 3 for the calculation of X(3). These produce results from the PDSP16510 representing bins 1, 5, 9, 13 etc.; followed by 2, 6, 10, 14 etc.; followed 3, 7, 11, 15 etc.

In order to sequentially output the final 4096 bins it is necessary to provide three FIFO's to store the various sets of results. These are then combined with the last set of results before being converted to phase and magnitude by the PDSP16330A.

The PDSP16318 performs the summation of four inputs, and a two bit word growth can occur. The two least significant bits are thus ignored by setting the shift control S2:0 to 010. The results from the four 1024 point transforms will have different scale tag values, and the results must be normalized to the largest set. This is done by detecting the minimum scale tag value and subtracting it from each of the other values. Each set of results is then shifted right by this amount using a PDSP1601.

These twiddles for the 4 point DFT can be combined with the window operator and the intermediate twiddle. This requires that the 4096 original window operators are arranged in four sets, each of which contains four groups of 1024 different values. Each operator in each group is then modified by $\exp(-j2\pi m/4)$ where n is the group number form 0 - 3. The four groups in each set are further modified by $\exp(-j2\pi ms/4096)$ where m = 0 -1023 and s = 0 in the first set, 1 in the second set, 2 in the third set, and 3 in the fourth set. This arrangement is illustrated in Figure 5.

The total PROM size must be 16384 words, addressed as four pages of 4096 words. The first page is used when the first points are being calculated using an address sequence of 0,1024, 2048, and 3072 ( to calculate the first point in the first DFT ); followed 1,1025,2049, 3073; and so on up to 1023, 2047, 3071, and 4095. The next page is then used to calculate all1024 second points of the DFT, then another page to calculate all the third points, and finally the last page is used to calculate all the fourth points.

**Performance**

The performance of the system is dictated by the time taken to do the following operations ; load the PDSP16510 with the results of the column DFT's, do a 1024 point transform, and then normalize and produce phase and magnitude outputs. These operations must be repeated for the calculation of every point in the column DFT. Since the maximum clock frequency of the PDSP support devices is 20 MHz, it will take 100 nanoseconds to calculate one point of a 2 point DFT, or 200 nanoseconds to calculate one point of a 4 point DFT, or 400 nanoseconds to calculate one point of an 8 point DFT, or 800 nanoseconds to do one point in a 16 point DFT.

Thus the time taken to load 1024 intermediate results into the PDSP16510 is 102.4 microseconds when 2 point DFT's are done. The transform time itself takes 97.7 microseconds with a 40 MHz system clock, and to this must be added the time to dump the results. It should be noted that the dump rate of the PDSP16510 can be solely dictated by the requirements of the system.

It will actually support dump rates of 40 MHz, and these rates can be sustained if each set of results is loaded into a 40 MHz FIFO ( not shown in Figure 4 ). The dump time is then only 25.6 microseconds as far as the performance calculation is concerned, and the total time needed to produce 2048 results is 2 x ( 102.4 + 97.7 + 25.6 ) = 451.4 microseconds. This corresponds to an input sampling rate of 4.5 MHz. It should be noted that the results need only be read out of each FIFO before the next load, transform, and FIFO write operation is complete i.e. data can be read out at the input sampling rate of 4.5 MHz. The combined rate going into the PDSP16330 is then 9 MHz, and standard grade parts can be used. From the complete system point of view, it might be more convenient if the output clock is obtained by dividing down the 40 MHz system clock needed by the PDSP16510. Either 5 or 10 MHz read rates could then be used, but an A grade PDSP16330 would be needed in the latter case.

This 4.5 MHz input sampling rate is the maximum sampling rate possible with this arrangement, and is only achievable when two 40 MHz output FIFO's are provided. Figure 4 , in fact, only shows the need for one output FIFO. In this situation the performance of the PDSP16330 and PDSP1601 limit the input sampling rate, and A grade parts should be used to allow 20 MHz outputs.The results from the second 1024 point transform can then only be dumped at 10 MHz, and are combined with the FIFO output to give a 20 MHz stream into the Pythagoras Processor. A more conservative performance figure is thus obtained if only one 20 MHz FIFO is assumed to be present, which results in a dump time of 51.2 microseconds for one transform and 102.4 microseconds for the other. The total 2048 point calculation time is then 553.8 microseconds, which corresponds to an input sampling rate of 3.7 MHz.

The above calculations are repeated for 4096, 8192, and 16384 point transforms and the results are summarized in Table 1. Both the maximum performance figures using two FIFO's, and the more conservative figures using one slower speed FIFO are given.

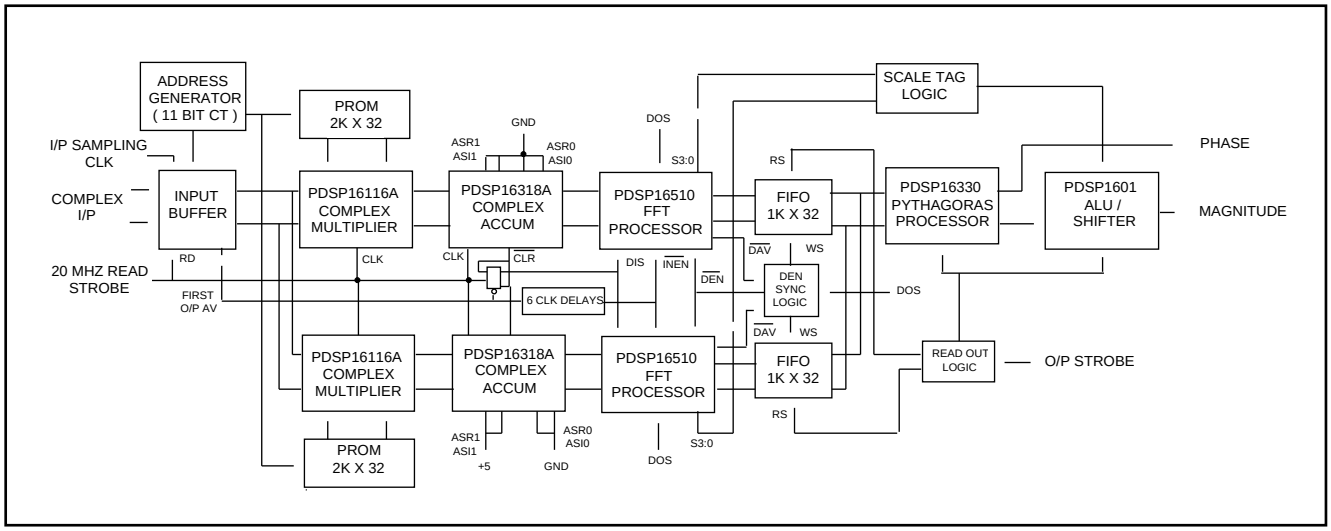


*Figure 6. A 2048 point system using two PDSP16510 devices for increased performance*

These performance figures can be improved by supplying a complete data path to compute each value in the DFT. Thus two data paths are needed to compute a 2048 point transform, four paths for a 4096 point transform, eight paths for a 8192 point transform, and 16 paths for a 16384 point transform. All the points in any given DFT are then produced simultaneously and applied to their own PDSP16510.

Figure 6 shows the use of two data paths in a 2048 point system, which will support sampling rates up to 9 MHz. These rates can be accomplished with only one PDSP16330A and one PDSP1601A. Because of internal synchronisation within the FFT Processor, one of the data paths may have finished its transform before the other. The paths can be pulled into synchronization by detecting when both DAV signals have gone active, and then generating a common DEN signal which has been synchronized to the DOS strobe. The slower read operations can commence as soon as the FIFO's are not empty. Alternatively both FIFO's can be allowed to fill in their own time , and data then read out when both are full. In this arrangement read and writes need not overlap, but sufficient space must be available in the FIFO's for the next set of results.

Figure 7 is a generic arrangement suitable for any number of data paths, which might be needed to sustain a particular sampling rate. It actually shows four data paths doing a 4096 point transform, with the results going into four FIFO's. These are then read out one after the other to give the sequential results of the 4096 point transform. The four sets of modified window operators are now split between four individual PROMS, but the total contents are the same. The results achieved are also summarized in Table1, and are given for FIFO's with both 40 MHz and 20 MHz writing rates. The reading rates needed are much lower, in fact the rate of combined data going into the PDSP16330 need only be the same as the input sampling rate. The reading rate of the individual FIFO's is proportionally less than this, and depends on the number of data paths in the system.

If the performance achieved with the full complement of additional data paths is too high, then the number of paths can be reduced to suite the sampling rates required.

This technique can be modified to perform 512 point transforms, with the PDSP16510 then doing 256 point complex transforms. In this mode load and dump operation can be concurrent with internal transform operations. With a 40 MHz system clock the transform time is 20.4 microseconds, but the load time is dictated by the 10 MHz maximum rate of producing DFT values from the PDSP16318. This results in a load time of 25.6 microseconds, which is greater than the transform time. The transform time is thus not the limiting factor, and it could be increased to 25.6 microseconds by using a slower system clock.The dump time can also be 25.6 microseconds without restraining the system level performance.

| | MAXIMUM SAMPLING RATES | | | |
|---|---|---|---|---|
| TRANSFORM SIZE | ONE DATA PATH | | L COMPLETE DATA PATHS | |
| | 20 MHz FIFO | 2 x 40 MHz FIFO | 20 MHz FIFO'S | 40MHz FIFO'S |
| 512 ( L = 2 ) | 10MHz | - - - - - - - - | 20 MHz | - - - - - - - - |
| 2048 ( L = 2 ) | 3.7 MHz | 4.7 MHz | 8.1 MHz | 9 MHz |
| 4096 ( L = 4 ) | 2.6 MHz | 3.1 MHz | 11.5 MHz | 12.4 MHz |
| 8192 ( L = 8 ) | 1.7 MHz | 1.9 MHz | 14.6 MHz | 15.3 MHz |
| 16384 ( L = 16 ) | 1 MHz | 1.08 MHz | 16.9 MHz | 17.3 MHz |

*Table 1. Maximum Sampling Rates*

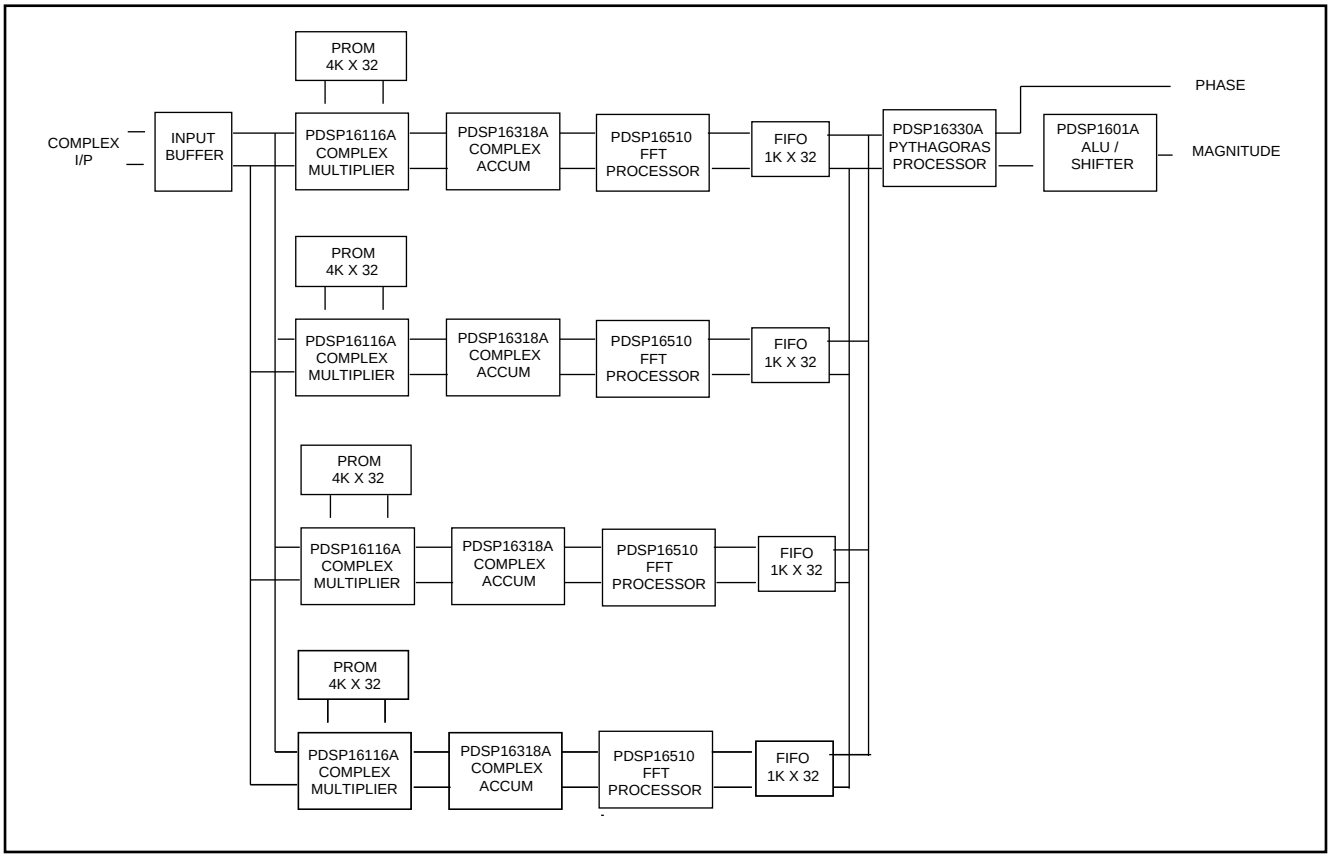


*Figure 7. A high performance 4096 point system using four complete data paths*

This level of perfromance can be sustained with only one FIFO to store the first set of results, and then dumping the second set of results at 10 MHz. The total time needed for the PDSP16510 to perform two 256 point transforms is thus 2 x 25.6 microseconds, which equates to an input sampling rate of 10 MHz. Two data paths would increase this sampling rate to 20 MHz.

**AB35**


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